## ABSTRACT

A filter coefficient adjusting circuit of the present invention comprises a coefficient adjusting circuit (2) that adjusts an equalization coefficient by weighting an initial value of the equalization coefficient on the left side from a center tap of a FIR filter (1) that equalizes a reproduce signal, by a factor of n, and weighting an initial value of the equalization coefficient on the right side by a factor of (2-n), and determines the factor n of the weighting so as to optimize an output of a jitter detector (5), for example, that detects jitter between the reproduced signal and a clock, as an equalization performance detecting means that detects an equalization performance of the reproduce signal.

According to the filter coefficient adjusting circuit of the present invention, it is possible to simplify the control method as compared to conventional group delay correcting circuits, and optimize the group delay of the reproduced signal according to the characteristics of the reproduced signal without requiring any additional circuits, thereby improving the reproduction performance.